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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/822,190	04/02/2001	Ronald J. Gagnon	85773-349	7309

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EXAMINER	
DOOLEY, MATTHEW C	
ART UNIT	**PAPER NUMBER**
2133	5

DATE MAILED: 03/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

7

Office Action Summary	Application No.	Applicant(s)	
	09/822,190	GAGNON, RONALD J.	
	Examiner	Art Unit	
	Matthew C. Dooley	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2,3,4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 1-3, 14-22 are rejected under 35 U.S.C. 101 because the claimed subject material invention lacks patentable utility.

As per claims 1-3, 14-22:

Claims 1 and 14 teach to a signal without structure that fails to provide a tangible process, machine, manufacture, or composition of matter. The claimed material constitutes an arrangement of data bits to be read or outputted, and as such, does not constitute patentable subject matter as required under 35 U.S.C. 101. Furthermore, claims 2-3 and 15-22 further limit the unpatentable independent claims 1 and 14 and, as such, are too rejected under the aforementioned reasoning.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-3 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 is directed to the use of forward correction data, however, gives no

structure, means, or method for the using of said data. As such, the applicant has failed to point out and distinctly claim the subject matter which applicant regards as the invention. Claim 2 specifies that the signal can pass between two circuits, however, there remains no inventive step, process, or structure claimed. Claim 3 further requires that the IC's be on a same circuit pack, but here too, there is no manipulation of the signal for a purpose, merely a claim suggesting a signal which may pass between two circuits. Here too, the applicant fails to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Bruce, Jr. et al., U.S. 5,517,637.

As per claim 1:

Bruce teaches to a forward error correction signal carried over a backplane (Col.6: 12-14).

As per claim 2:

The system of Bruce teaches to an ECC data signal carried over a link between two integrated circuits (Col.6: 1-31; Col.7: 4-8, 21-24).

As per claim 3:

The multiple circuits of Bruce that are tested by the forward error correction signal are included on the same circuit pack (Col.6: 9-50).

6. Claim 4, 7-9, 12-14, 17-21 is rejected under 35 U.S.C. 102(e) as being anticipated by Fujisawa et al., U.S. 6,657,967.

As per claim 4:

Fujisawa teaches to an input for receiving an input signal comprising a payload to be transmitted between two IC's, a processing unit for processing the payload data to derive FEC data on the basis of the payload data in the input signal and generating an output signal comprising payload and FEC data, and an output for outputting the signal over a link between two IC's (Fig.1).

As per claim 7:

Fujisawa teaches processing unit for processing the input signal to generate primary data structures comprising a first data and second error correction portion derived from the first portion (Fig.1,3). Also taught is a multiplexing function to derive a data structure, frame generation and output signal generation (Fig.1,4,5,6).

As per claim 8:

Fujisawa teaches to an input for receiving an input signal comprising a data to be transmitted between two IC's, a processing unit for processing the data into frames of

sequential blocks with payload data and overhead information, a multiplexing function to derive a data structure from data comprising payload and FEC data based on the payload data, frame generation and output signal generation (Fig.1,3,4,5,6).

As per claim 9:

Claim 9 is the corresponding method claim to apparatus claim 4 and as such claim 9 can be rejected using analogous reasoning to that used in the rejection of claim 4 above.

As per claim 12:

Claim 12 is the corresponding method claim to apparatus claim 7 and as such claim 12 can be rejected using analogous reasoning to that used in the rejection of claim 7 above.

As per claim 13:

Claim 13 is the corresponding method claim to apparatus claim 8 and as such claim 13 can be rejected using analogous reasoning to that used in the rejection of claim 8 above.

As per claim 14:

Fujisawa teaches to an input for receiving an input signal comprising a data to be transmitted between two IC's, wherein the signal includes frames of sequential blocks with payload data and overhead information, a multiplexing function to derive a data structure from data comprising payload and FEC data based on the payload data, frame generation and output signal generation (Fig.1,3,4,5,6).

As per claim 17:

The number of primary data structures in the system of Fujisawa is about 4 (Fig.6).

As per claim 18:

The rate of the signal of Fujisawa is about 2.5 Gb/s (Col.2: 24-26).

As per claim 19:

Fujisawa teaches to sequential blocks and a framing pattern(Fig.2-6).

As per claim 20:

Fujisawa teaches to a primary data structure about of size 1176 bits (Fig.2-6).

As per claim 21:

Fujisawa teaches that the signal contains payload and a short FEC data segment (Fig.5).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 5, 10, 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujisawa et al., U.S. 6,657,967, in view of Bruce, Jr. et al., U.S. 5,517,637.

As per claim 5:

It is unclear that the system of Fujisawa operates on a single backplane. Bruce teaches that FEC signals can pass between two circuits on a backplane(Col.6: 1-50;

Col.7: 4-8, 21-24).. As such, it would have been obvious for one of ordinary skill in the art to make use of the backplane technology of Bruce in conjunction with the system of Fujisawa because the use of a single backplane allows for the circuitry of Fujisawa to be manufactured on a single backplane.

As per claim 10:

Claim 10 is the corresponding method claim to apparatus claim 5 and as such claim 10 can be rejected using analogous reasoning to that used in the rejection of claim 5 above.

As per claim 15:

It is unclear that the system of Fujisawa operates on a single circuit pack. Bruce teaches that FEC signals can pass between two circuits on a circuit pack (Col.6: 1-50; Col.7: 4-8, 21-24).. As such, it would have been obvious for one of ordinary skill in the art to make use of the backplane technology of Bruce in conjunction with the system of Fujisawa because the use of a single backplane allows for the circuitry of Fujisawa to be manufactured on a single circuit pack.

As per claim 16:

It is unclear that the system of Fujisawa operates on a single circuit pack. Bruce teaches that FEC signals can pass between two circuits on a circuit pack (Col.6: 1-50; Col.7: 4-8, 21-24).. As such, it would have been obvious for one of ordinary skill in the art to make use of the backplane technology of Bruce in conjunction with the system of Fujisawa because the use of a single backplane allows for the circuitry of Fujisawa to be manufactured on a single circuit pack.

9. Claim 6, 11, 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujisawa et al., U.S. 6,657,967, in view of Wolf, U.S. 6,061,825.

As per claim 6:

The system of Fujisawa does not explicitly claim a FEC method, but rather allows for any type of forward error correction. Wolf teaches to the use of BCH coding on data. It would have been obvious to one of ordinary skill in the art at the time of the invention to make use of BCH decoding in the system of Fujisawa because BCH coding is a well known method of error coding that allows for robust error detection and correction (Wolf: Col.2: 5-15).

As per claim 11:

Claim 11 is the corresponding method claim to apparatus claim 6 and as such claim 11 can be rejected using analogous reasoning to that used in the rejection of claim 6 above.

As per claim 22:

The system of Fujisawa does not explicitly claim a FEC method, but rather allows for any type of forward error correction. Wolf teaches to the use of BCH coding on data. It would have been obvious to one of ordinary skill in the art at the time of the invention to make use of BCH decoding in the system of Fujisawa because BCH coding is a well known method of error coding that allows for robust error detection and correction (Wolf: Col.2: 5-15).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Dooley whose telephone number is (703) 306-5538. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew Dooley
Examiner AU 2133
04/08/04

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